Fig. 1 PRIOR ART

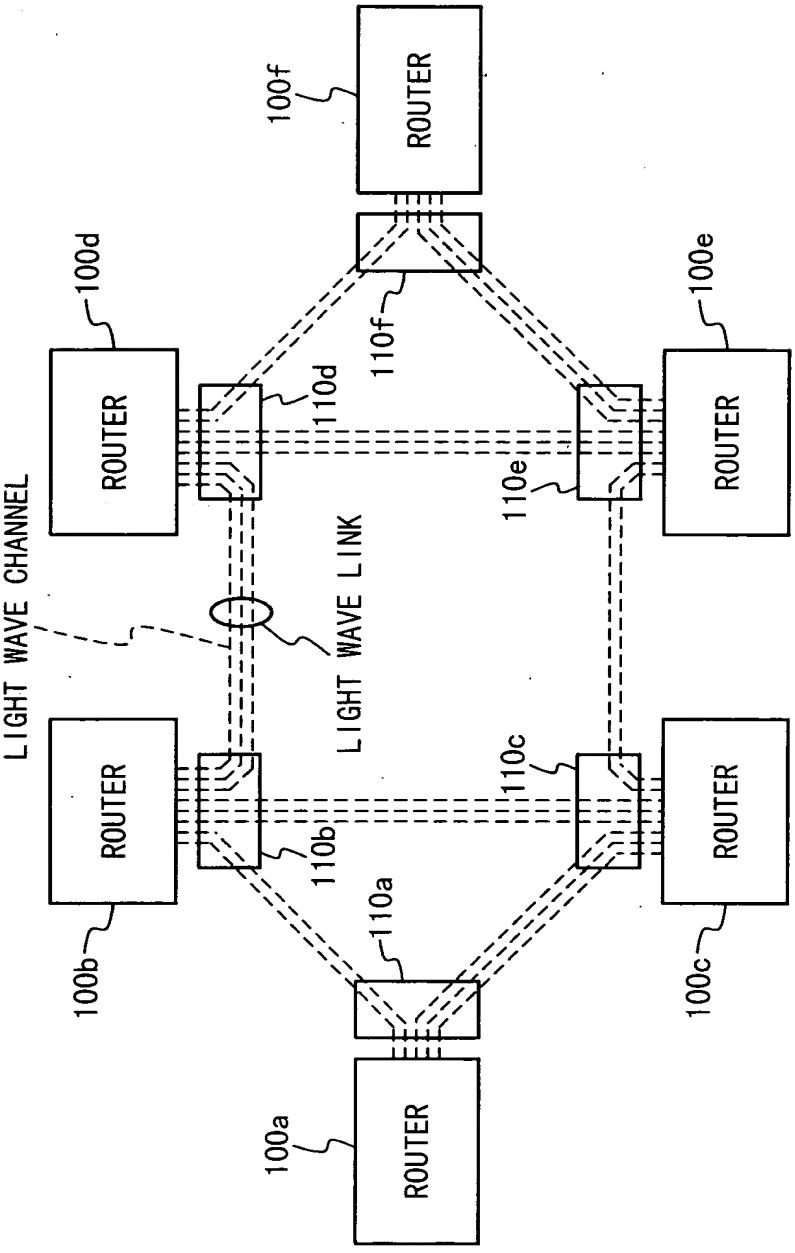

Fig. 2 PRIOR ART

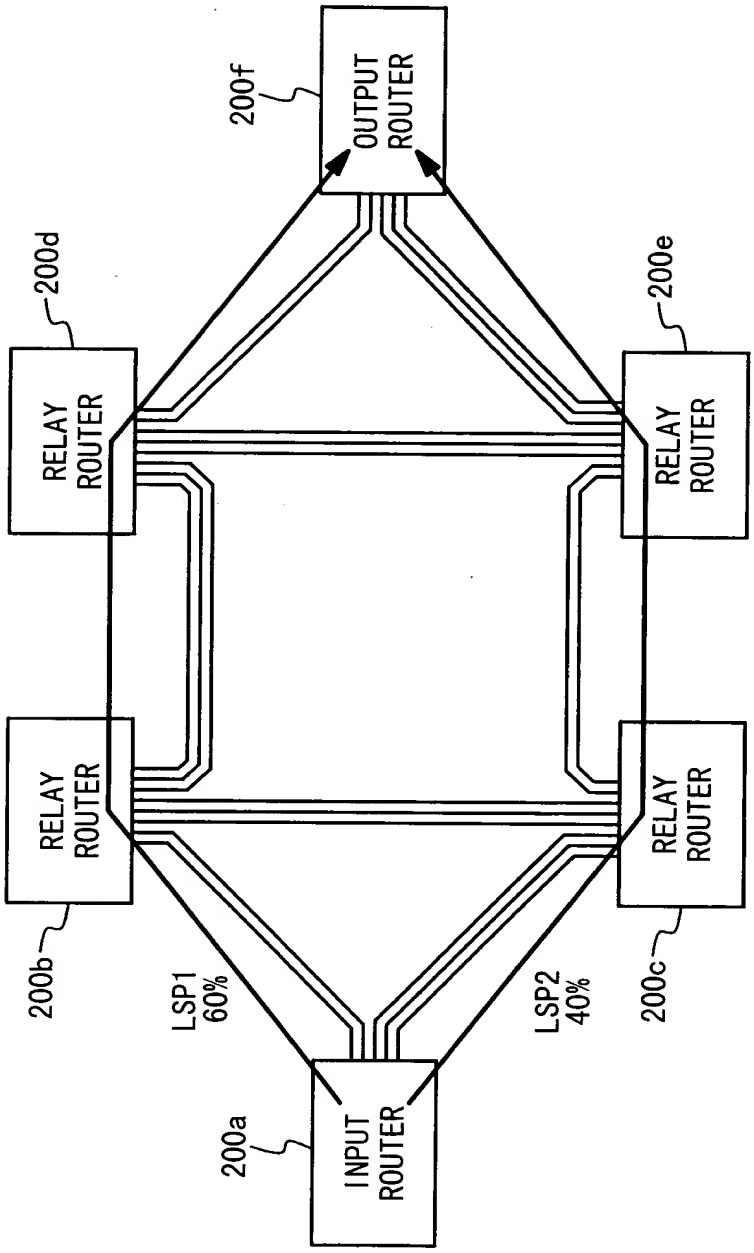

Fig. 3 PRIOR ART

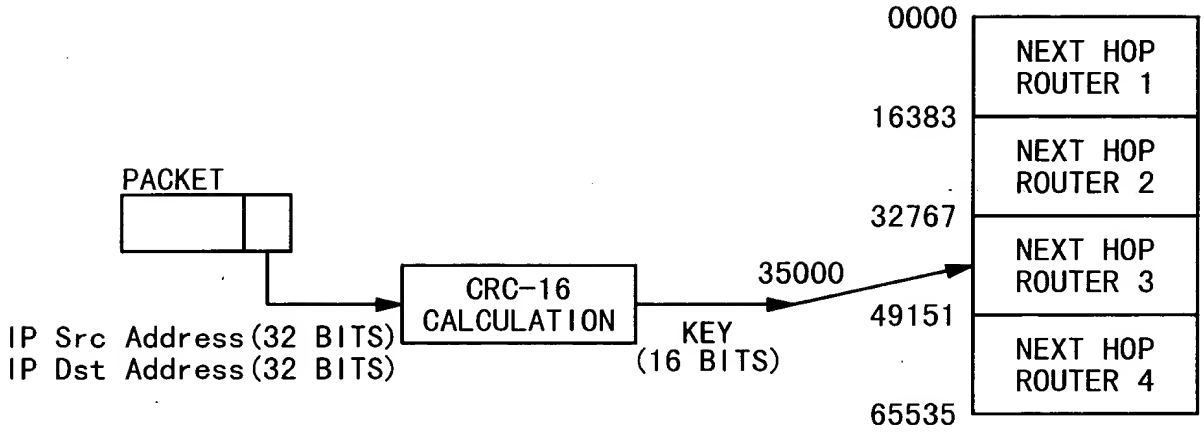

Fig. 4A PRIOR ART

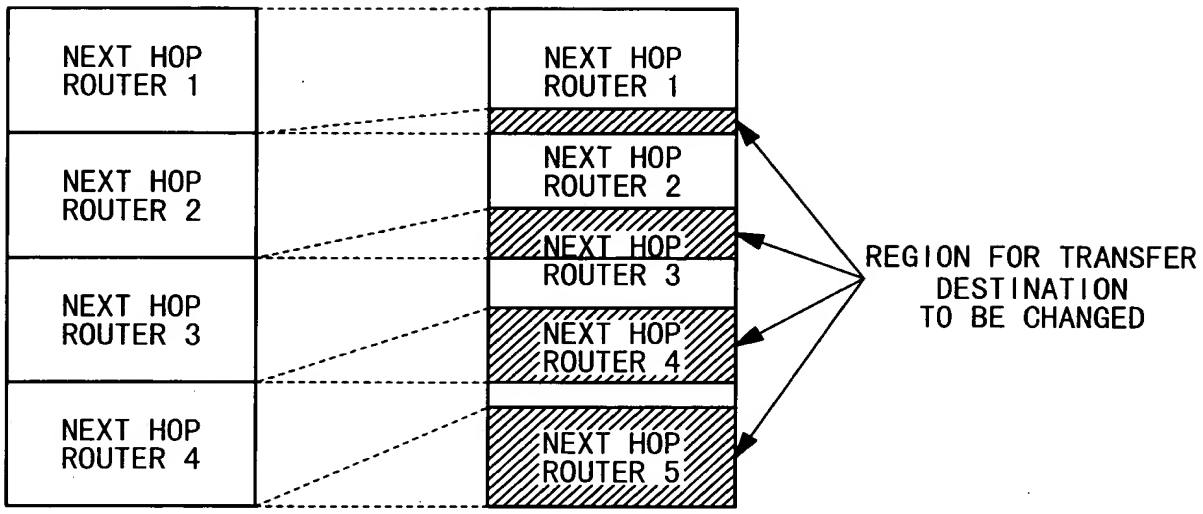

Fig. 4B PRIOR ART

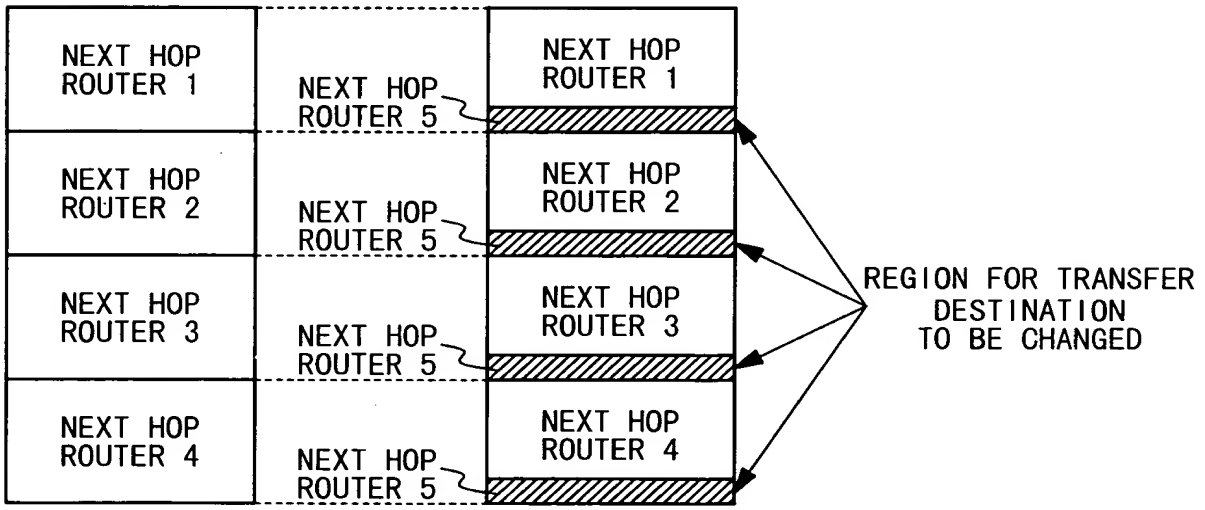

Fig. 5

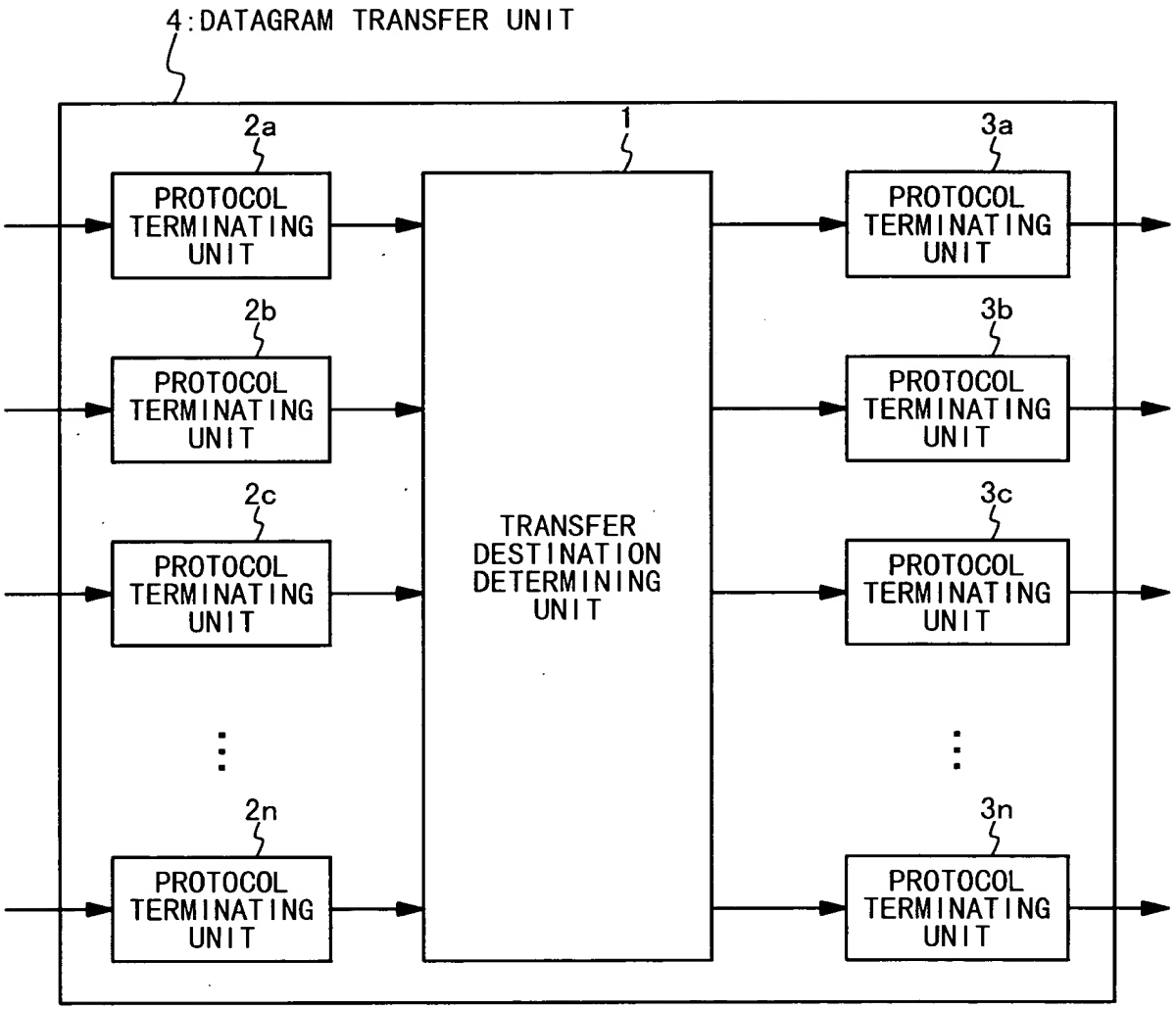
4:DATAGRAM TRANSFER UNIT
2a
PROTOCOL TERMINATING UNIT
2b
PROTOCOL TERMINATING UNIT
2c
PROTOCOL TERMINATING UNIT
2n
PROTOCOL TERMINATING UNIT
1
TRANSFER DESTINATION DETERMINING UNIT
3a
PROTOCOL TERMINATING UNIT
3b
PROTOCOL TERMINATING UNIT
3c
PROTOCOL TERMINATING UNIT
3n
PROTOCOL TERMINATING UNIT

Fig. 6

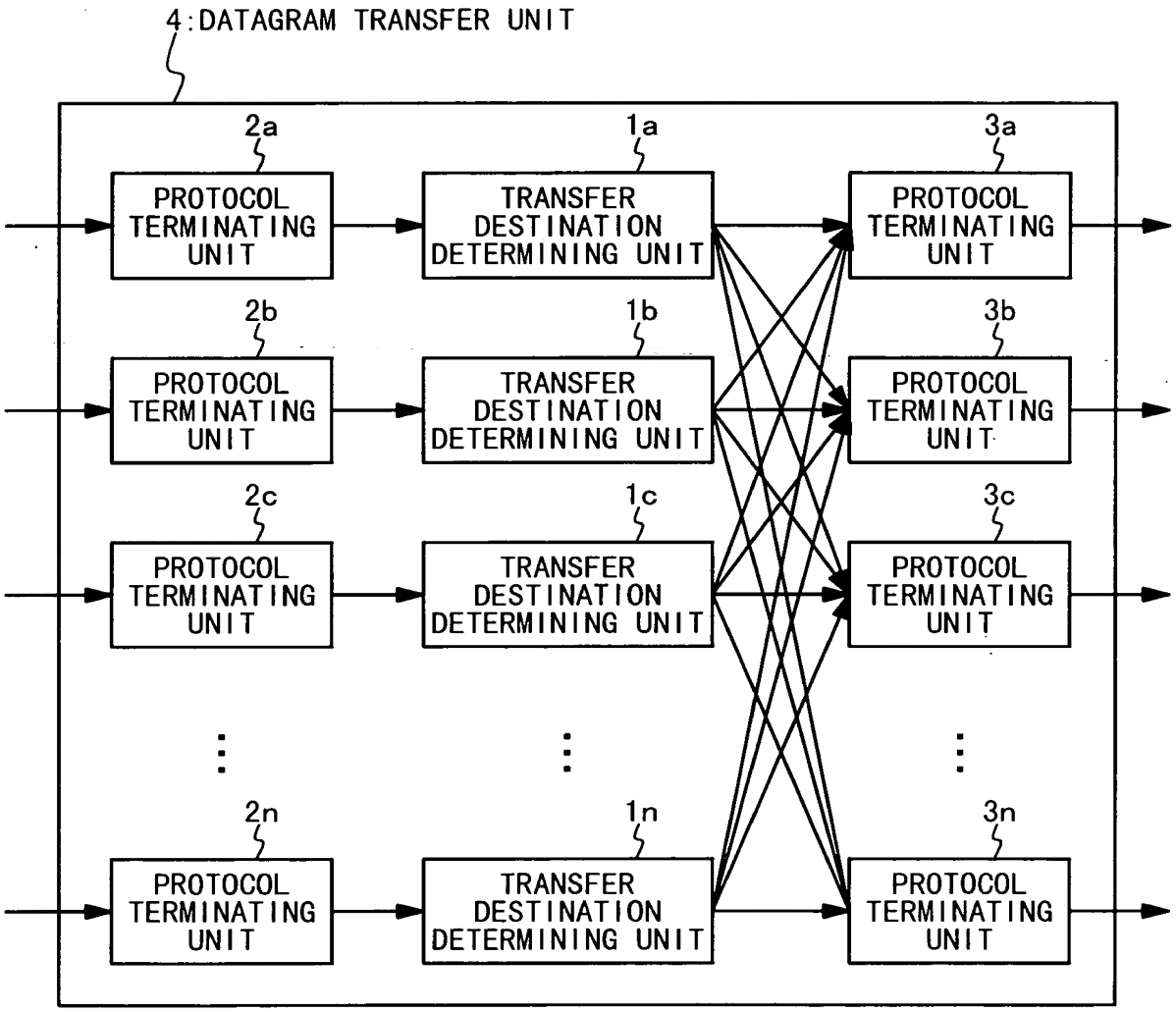
4:DATAGRAM TRANSFER UNIT
2a
1a
3a
PROTOCOL TERMINATING UNIT
TRANSFER DESTINATION DETERMINING UNIT
PROTOCOL TERMINATING UNIT
2b
1b
3b
PROTOCOL TERMINATING UNIT
TRANSFER DESTINATION DETERMINING UNIT
PROTOCOL TERMINATING UNIT
2c
1c
3c
PROTOCOL TERMINATING UNIT
TRANSFER DESTINATION DETERMINING UNIT
PROTOCOL TERMINATING UNIT
2n
1n
3n
PROTOCOL TERMINATING UNIT
TRANSFER DESTINATION DETERMINING UNIT
PROTOCOL TERMINATING UNIT

Fig. 7

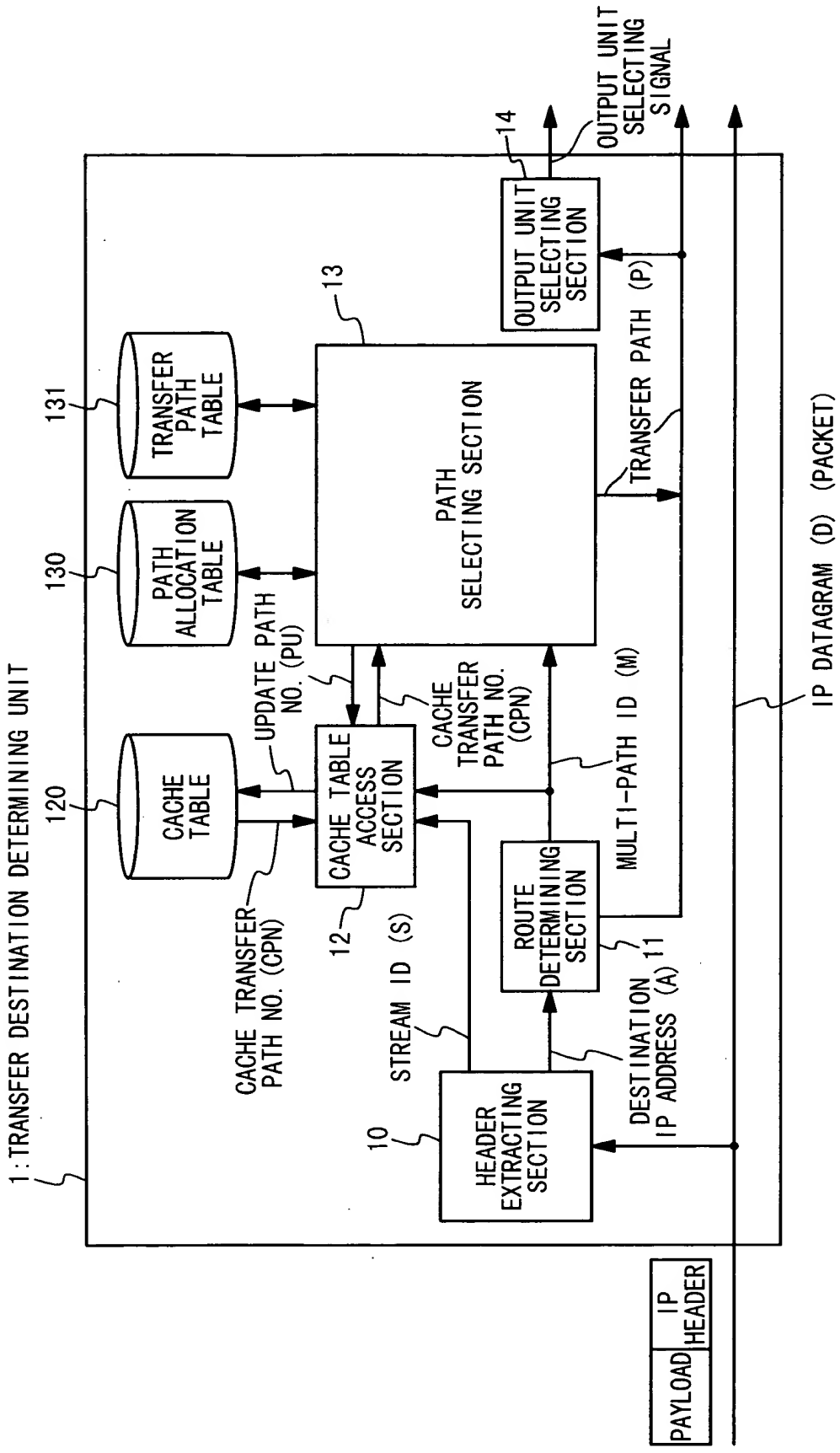
1: TRANSFER DESTINATION DETERMINING UNIT
HEADER EXTRACTING SECTION
10
STREAM ID (S)
DESTINATION IP ADDRESS (A)
ROUTE DETERMINING SECTION
11
CACHE TABLE ACCESS SECTION
12
CACHE TRANSFER PATH NO. (CPN)
UPDATE PATH NO. (PU)
CACHE TABLE
120
PATH ALLOCATION TABLE
130
TRANSFER PATH TABLE
131
PATH SELECTING SECTION
13
CACHE TRANSFER PATH NO. (CPN)
MULTI-PATH ID (M)
TRANSFER PATH (P)
OUTPUT UNIT SELECTING SECTION
14
OUTPUT UNIT SELECTING SIGNAL
IP DATAGRAM (D) (PACKET)
IP HEADER
PAYLOAD

Fig. 8

120:CACHE TABLE

ADDRESS SECTION		DATA SECTION
MULTI-PATH ID (M)	STREAM ID (S)	CACHE TRANSFER PATH NO. (CPN)
	000	1
	001	2
	002	0
	003	NON REGISTERED
0	004	NON REGISTERED
	005	0
	⋮	⋮
	FFF	3
	000	1
1	001	NON REGISTERED
	002	2

Fig. 9

130:PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION			
MULTI-PATH ID (M)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	00000000	00000000	1	1
1	11110000	11110000	2	2
2	11110010	11110010	3	0
3	11111001	11111001	3	0

⋮ CORRESPONDING TO PN = 7 ⋮

CORRESPONDING TO PN = 0

Fig. 10

131: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)	TRANSFER PATH (P)
0	0	600	3×256	3	PATH 0-0
	1	650	3×256	3	PATH 0-1
	2	1000	5×256	5	PATH 0-2
	3	1200	5×256	5	PATH 0-3
	4	0	0	0	NONE
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE
1	0	1500	6×256	1	PATH 1-0
	1				
	2				
	3				

Document Processing Unit

Fig. 11

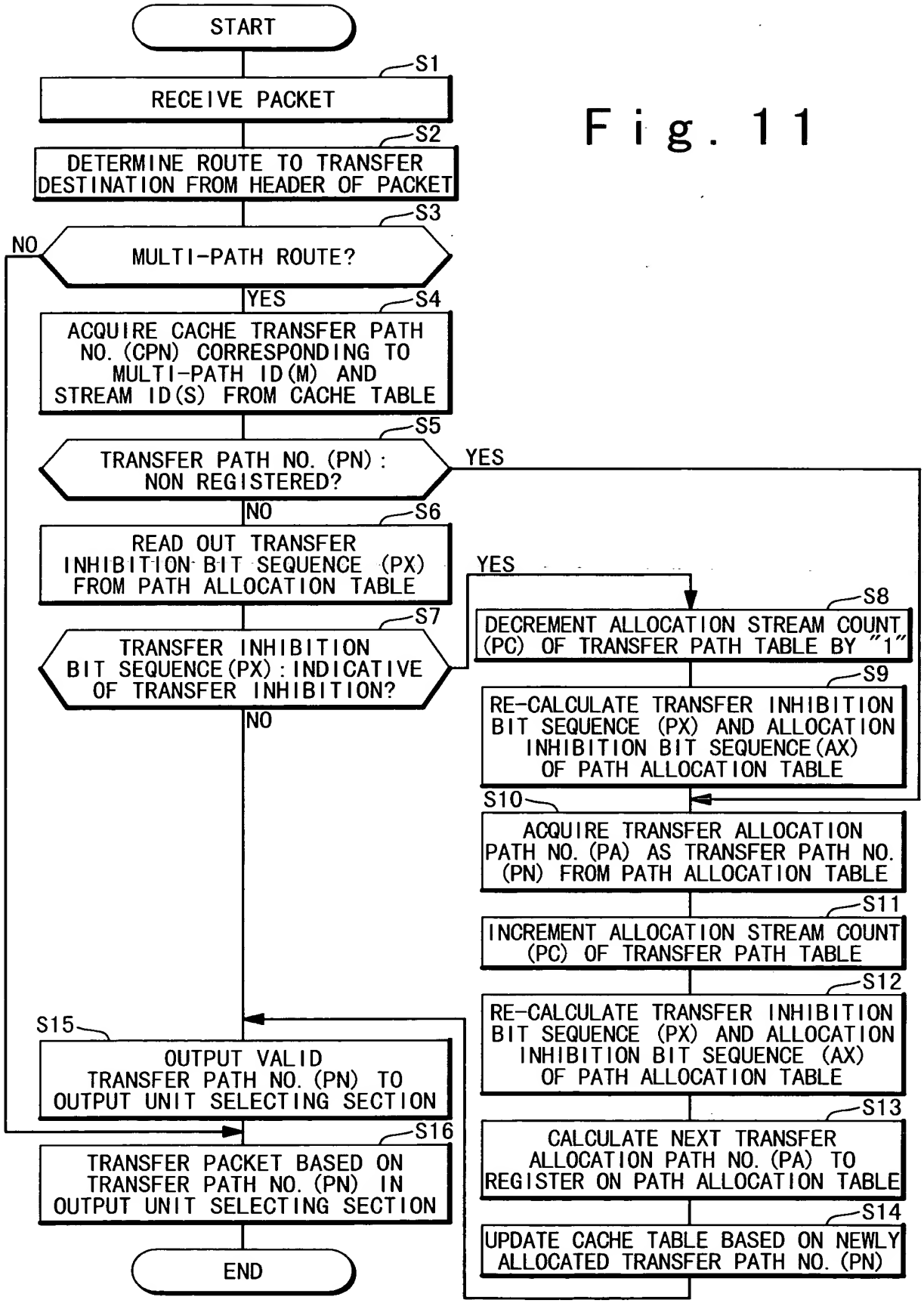
START
S1
RECEIVE PACKET
S2
DETERMINE ROUTE TO TRANSFER DESTINATION FROM HEADER OF PACKET
S3
MULTI-PATH ROUTE?
NO
YES
S4
ACQUIRE CACHE TRANSFER PATH NO. (CPN) CORRESPONDING TO MULTI-PATH ID(M) AND STREAM ID(S) FROM CACHE TABLE
S5
TRANSFER PATH NO. (PN): NON REGISTERED?
YES
NO
S6
READ OUT TRANSFER INHIBITION BIT SEQUENCE (PX) FROM PATH ALLOCATION TABLE
S7
TRANSFER INHIBITION BIT SEQUENCE(PX): INDICATIVE OF TRANSFER INHIBITION?
YES
NO
S8
DECREMENT ALLOCATION STREAM COUNT (PC) OF TRANSFER PATH TABLE BY "1"
S9
RE-CALCULATE TRANSFER INHIBITION BIT SEQUENCE (PX) AND ALLOCATION INHIBITION BIT SEQUENCE(AX) OF PATH ALLOCATION TABLE
S10
ACQUIRE TRANSFER ALLOCATION PATH NO. (PA) AS TRANSFER PATH NO. (PN) FROM PATH ALLOCATION TABLE
S11
INCREMENT ALLOCATION STREAM COUNT (PC) OF TRANSFER PATH TABLE
S12
RE-CALCULATE TRANSFER INHIBITION BIT SEQUENCE (PX) AND ALLOCATION INHIBITION BIT SEQUENCE (AX) OF PATH ALLOCATION TABLE
S13
CALCULATE NEXT TRANSFER ALLOCATION PATH NO. (PA) TO REGISTER ON PATH ALLOCATION TABLE
S14
UPDATE CACHE TABLE BASED ON NEWLY ALLOCATED TRANSFER PATH NO. (PN)
S15
OUTPUT VALID TRANSFER PATH NO. (PN) TO OUTPUT UNIT SELECTING SECTION
S16
TRANSFER PACKET BASED ON TRANSFER PATH NO. (PN) IN OUTPUT UNIT SELECTING SECTION
END

Fig. 12

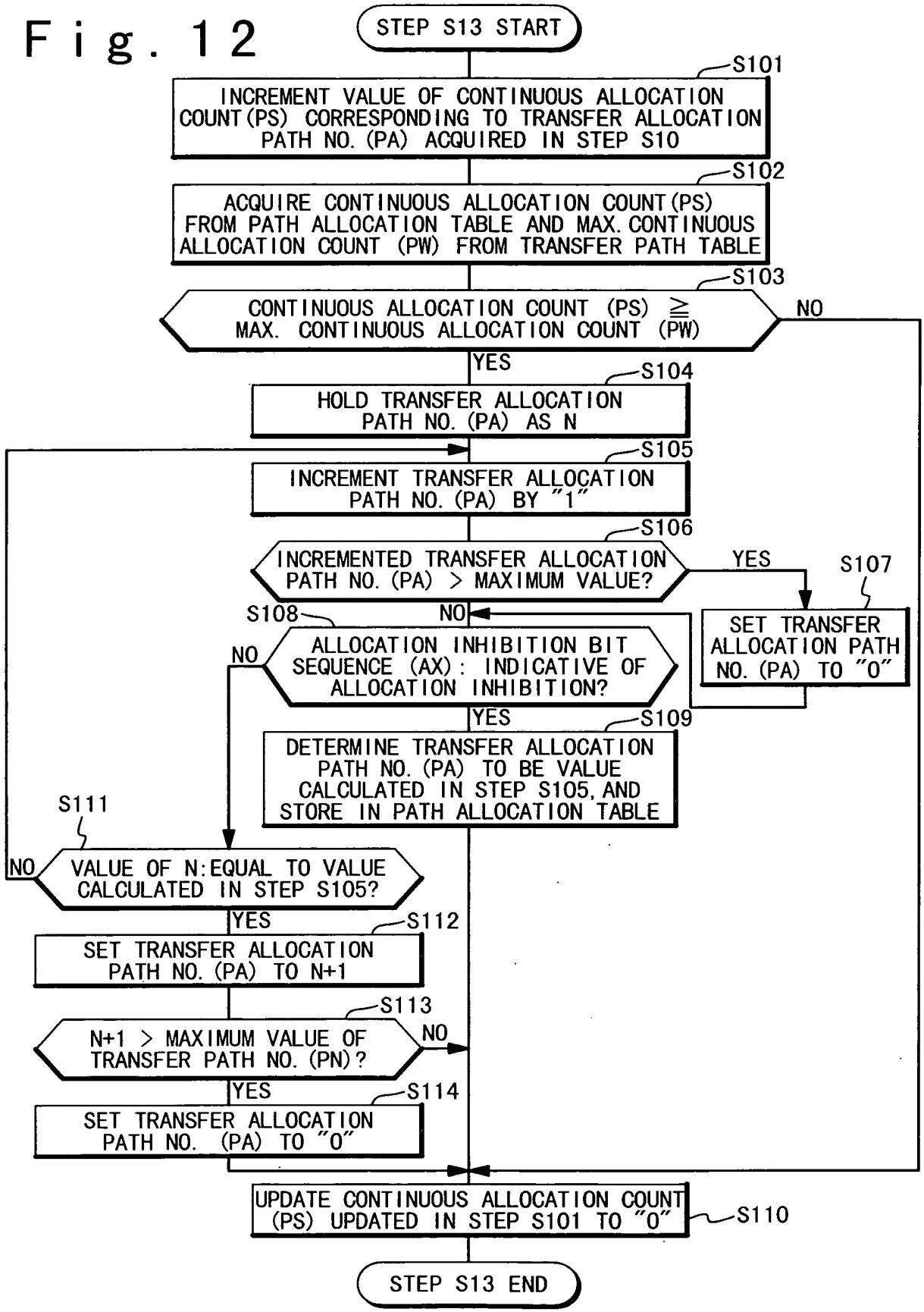
STEP S13 START
S101
INCREMENT VALUE OF CONTINUOUS ALLOCATION COUNT(PS) CORRESPONDING TO TRANSFER ALLOCATION PATH NO. (PA) ACQUIRED IN STEP S10
S102
ACQUIRE CONTINUOUS ALLOCATION COUNT(PS) FROM PATH ALLOCATION TABLE AND MAX. CONTINUOUS ALLOCATION COUNT (PW) FROM TRANSFER PATH TABLE
S103
CONTINUOUS ALLOCATION COUNT (PS) ≧ MAX. CONTINUOUS ALLOCATION COUNT (PW)
NO
YES
S104
HOLD TRANSFER ALLOCATION PATH NO. (PA) AS N
S105
INCREMENT TRANSFER ALLOCATION PATH NO. (PA) BY "1"
S106
INCREMENTED TRANSFER ALLOCATION PATH NO. (PA) > MAXIMUM VALUE?
YES
S107
SET TRANSFER ALLOCATION PATH NO. (PA) TO "0"
S108
NO
ALLOCATION INHIBITION BIT SEQUENCE (AX): INDICATIVE OF ALLOCATION INHIBITION?
NO
YES
S109
DETERMINE TRANSFER ALLOCATION PATH NO. (PA) TO BE VALUE CALCULATED IN STEP S105, AND STORE IN PATH ALLOCATION TABLE
S111
NO
VALUE OF N:EQUAL TO VALUE CALCULATED IN STEP S105?
YES
S112
SET TRANSFER ALLOCATION PATH NO. (PA) TO N+1
S113
N+1 > MAXIMUM VALUE OF TRANSFER PATH NO. (PN)?
NO
YES
S114
SET TRANSFER ALLOCATION PATH NO. (PA) TO "0"
UPDATE CONTINUOUS ALLOCATION COUNT (PS) UPDATED IN STEP S101 TO "0"
S110
STEP S13 END

Fig. 13

130:PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION			
MULTI-PATH ID (M)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	11100000	11100000	0	0

Fig. 14

131:TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)	TRANSFER PATH (P)
0	0	0	2×256	2	PATH 0-0
	1	0	3×256	3	PATH 0-1
	2	0	5×256	5	PATH 0-2
	3	0	5×256	5	PATH 0-3
	4	0	1×256	1	PATH 0-4
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE

Fig. 15

130:PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION			
MULTI-PATH ID (M)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	11100000	11111111	-	-

Fig. 16

131: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)	TRANSFER PATH (P)
0	0	2×256	2×256	0	PATH 0-0
	1	3×256	3×256	0	PATH 0-1
	2	5×256	5×256	0	PATH 0-2
	3	5×256	5×256	0	PATH 0-3
	4	1×256	1×256	0	PATH 0-4
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE

Fig. 17

130: PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION			
MULTI-PATH ID (M)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	11001100	11001110	0	0

Fig. 18

131: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)	TRANSFER PATH (P)
0	0	2×256	4×256	2	PATH 0-0
	1	3×256	3×256	0	PATH 0-1
	2	5×256	3×256	0	PATH 0-2
	3	5×256	0	0	(PATH 0-3)
	4	1×256	4×256	3	PATH 0-4
	5	0	1×256	1	PATH 0-5
	6	0	0	0	NONE
	7	0	0	0	NONE

Fig. 19

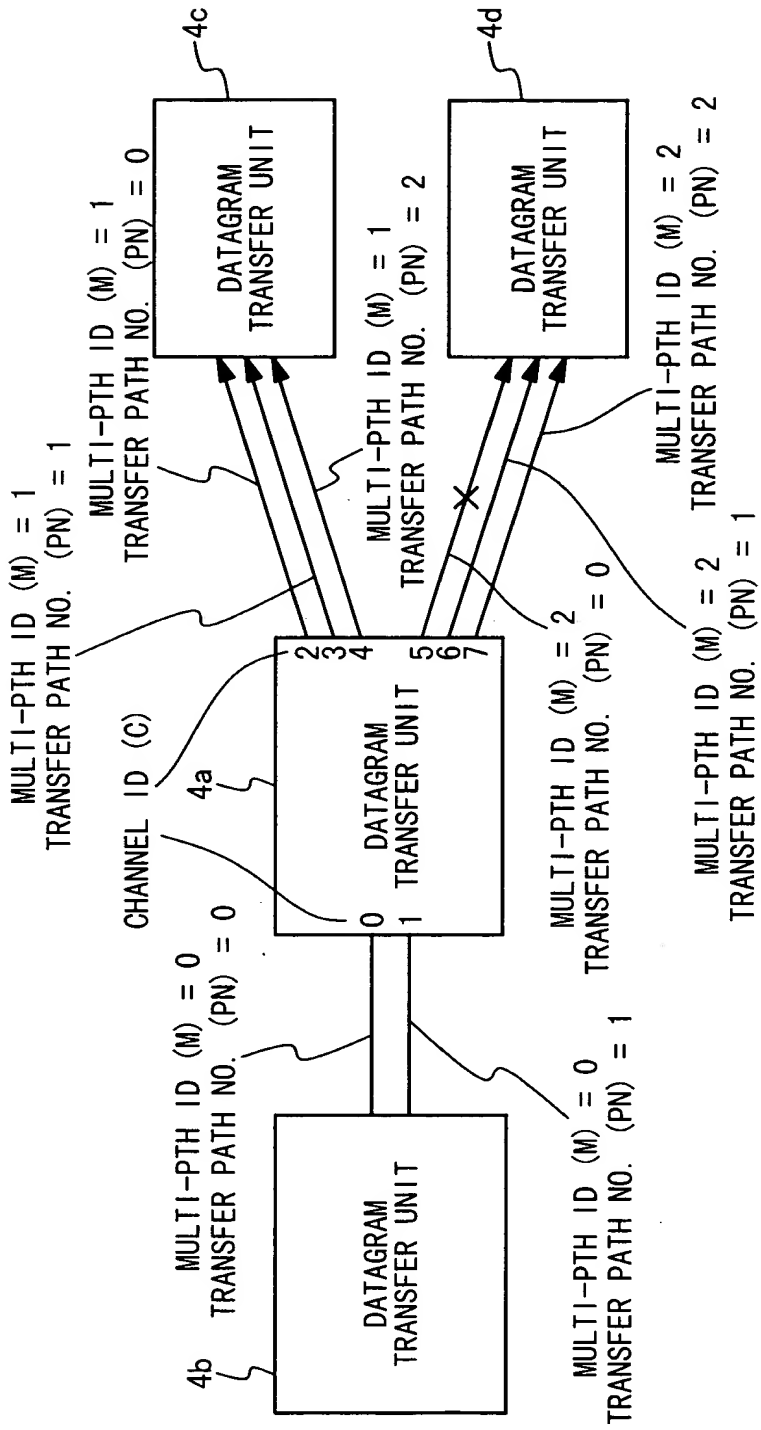
4c
4d
DATAGRAM TRANSFER UNIT
DATAGRAM TRANSFER UNIT
DATAGRAM TRANSFER UNIT
4a
4b
MULTI-PTH ID (M) = 1
TRANSFER PATH NO. (PN) = 0
MULTI-PTH ID (M) = 1
TRANSFER PATH NO. (PN) = 1
MULTI-PTH ID (M) = 1
TRANSFER PATH NO. (PN) = 2
MULTI-PTH ID (M) = 2
TRANSFER PATH NO. (PN) = 2
MULTI-PTH ID (M) = 2
TRANSFER PATH NO. (PN) = 1
MULTI-PTH ID (M) = 2
TRANSFER PATH NO. (PN) = 0
MULTI-PTH ID (M) = 0
TRANSFER PATH NO. (PN) = 0
MULTI-PTH ID (M) = 0
TRANSFER PATH NO. (PN) = 1
CHANNEL ID (C)
0
1
2
3
4
5
6
7

Fig. 20

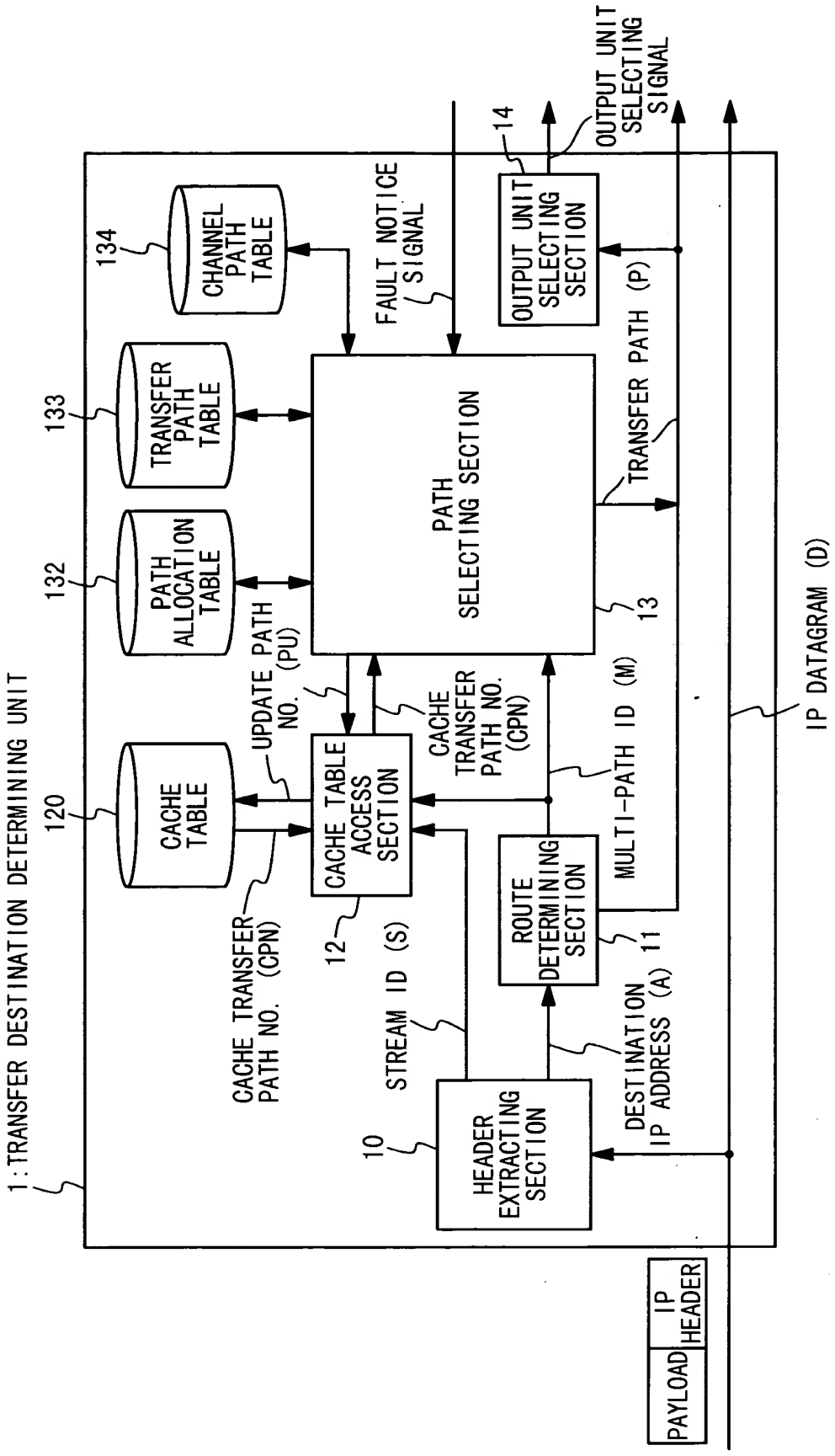
1: TRANSFER DESTINATION DETERMINING UNIT
IP DATAGRAM (D)
PAYLOAD
IP HEADER
HEADER EXTRACTING SECTION
10
DESTINATION IP ADDRESS (A)
STREAM ID (S)
ROUTE DETERMINING SECTION
11
MULTI-PATH ID (M)
CACHE TABLE ACCESS SECTION
12
CACHE TRANSFER PATH NO. (CPN)
CACHE TRANSFER PATH NO. (CPN)
UPDATE PATH NO. (PU)
CACHE TABLE
120
PATH SELECTING SECTION
13
TRANSFER PATH (P)
OUTPUT UNIT SELECTING SECTION
14
OUTPUT UNIT SELECTING SIGNAL
FAULT NOTICE SIGNAL
PATH ALLOCATION TABLE
132
TRANSFER PATH TABLE
133
CHANNEL PATH TABLE
134

Fig. 21

134: CHANNEL PATH TABLE

ADDRESS SECTION	DATA SECTION	
CHANNEL ID (C)	MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)
0	0	0
1	0	1
2	1	0
3	1	1
4	1	2
5	2	0
6	2	1
7	2	2

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Fig. 22

132:PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION					
MULTI-PATH ID (M)	OPERATION MODE (AM)	TRANSFER PATH STATUS BIT SEQUENCE (PD)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	NORMAL	11111100	11111100	11111111	0	0
1	NORMAL	11111000	11111000	11111111	0	0
2	NORMAL	11111000	11111000	11111111	0	0

Fig. 23

133: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)	TRANSFER PATH (P)
0	0	2048	2048	1	PATH 0-0
	1	2048	2048	1	PATH 0-1
	2	0	0	0	NONE
	3	0	0	0	NONE
	4	0	0	0	NONE
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE
1	0	1365	1365	1	PATH 1-0
	1	1365	1365	1	PATH 1-1
	2	1366	1366	1	PATH 1-2
	3	0	0	0	NONE
	4	0	0	0	NONE
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE
2	0	1365	1365	1	PATH 2-0
	1	1365	1365	1	PATH 2-1
	2	1366	1366	1	PATH 2-2
	3	0	0	0	NONE
	4	0	0	0	NONE
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE

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Fig. 24

132:PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION					
MULTI-PATH ID (M)	OPERATION MODE (AM)	TRANSFER PATH STATUS BIT SEQUENCE (PD)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	NORMAL	11111100	11111100	11111111	0	0
1	NORMAL	11111000	11111000	11111111	0	0
2	FAULT STATE	11111001	11111000	11111111	0	0

Fig. 25

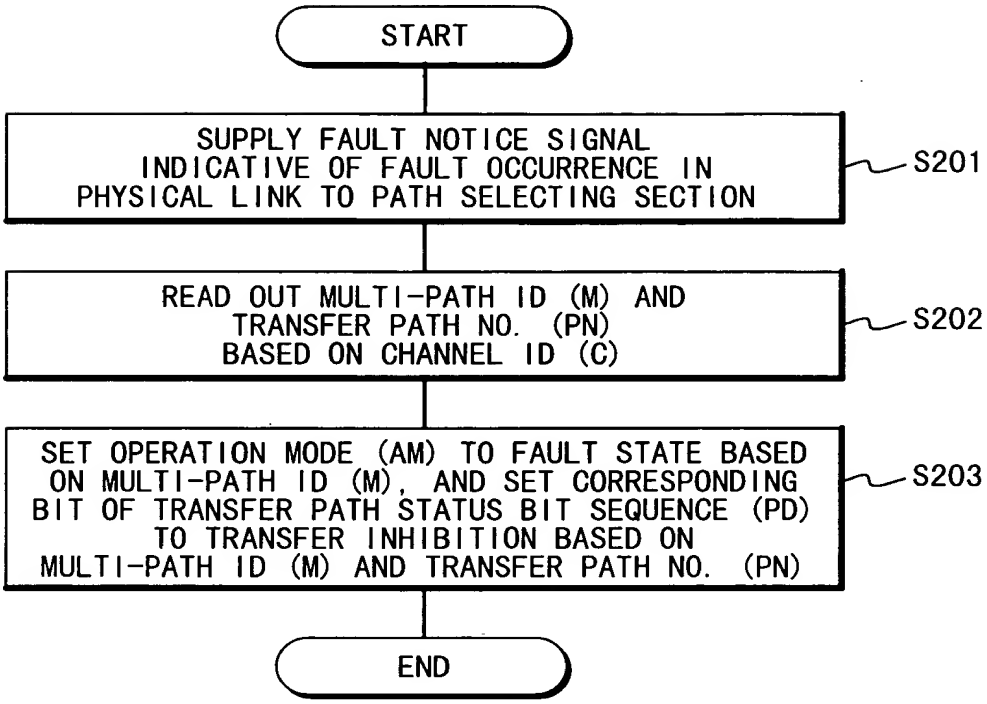

START
SUPPLY FAULT NOTICE SIGNAL INDICATIVE OF FAULT OCCURRENCE IN PHYSICAL LINK TO PATH SELECTING SECTION
S201
READ OUT MULTI-PATH ID (M) AND TRANSFER PATH NO. (PN) BASED ON CHANNEL ID (C)
S202
SET OPERATION MODE (AM) TO FAULT STATE BASED ON MULTI-PATH ID (M), AND SET CORRESPONDING BIT OF TRANSFER PATH STATUS BIT SEQUENCE (PD) TO TRANSFER INHIBITION BASED ON MULTI-PATH ID (M) AND TRANSFER PATH NO. (PN)
S203
END

Fig. 26

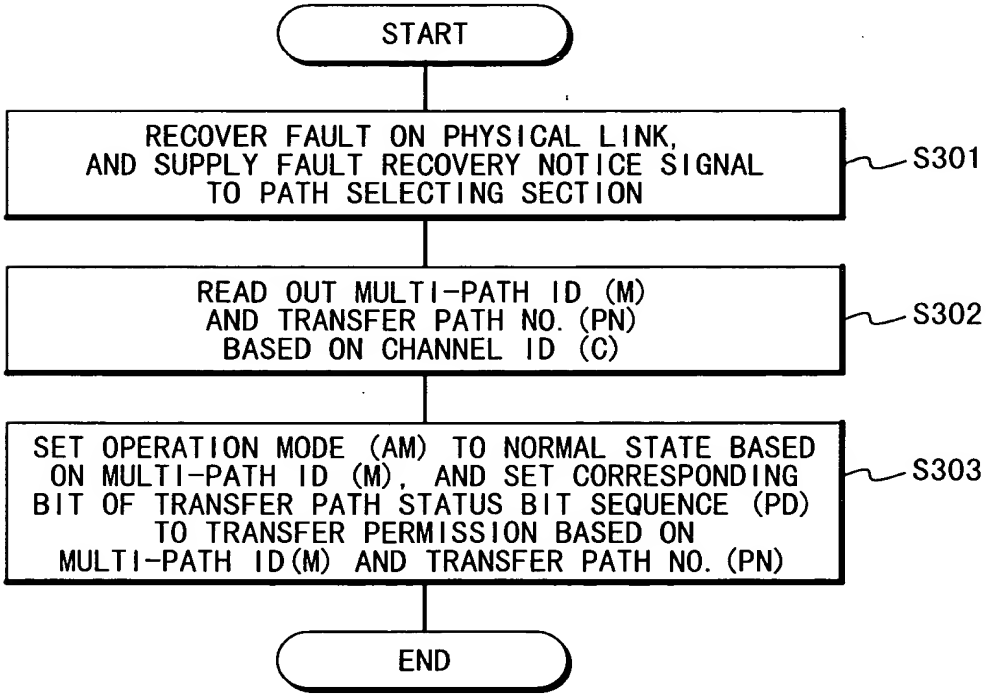

START
RECOVER FAULT ON PHYSICAL LINK, AND SUPPLY FAULT RECOVERY NOTICE SIGNAL TO PATH SELECTING SECTION
S301
READ OUT MULTI-PATH ID (M) AND TRANSFER PATH NO. (PN) BASED ON CHANNEL ID (C)
S302
SET OPERATION MODE (AM) TO NORMAL STATE BASED ON MULTI-PATH ID (M), AND SET CORRESPONDING BIT OF TRANSFER PATH STATUS BIT SEQUENCE (PD) TO TRANSFER PERMISSION BASED ON MULTI-PATH ID(M) AND TRANSFER PATH NO. (PN)
S303
END

Fig. 27A

Fig. 27
Fig. 27A
Fig. 27B

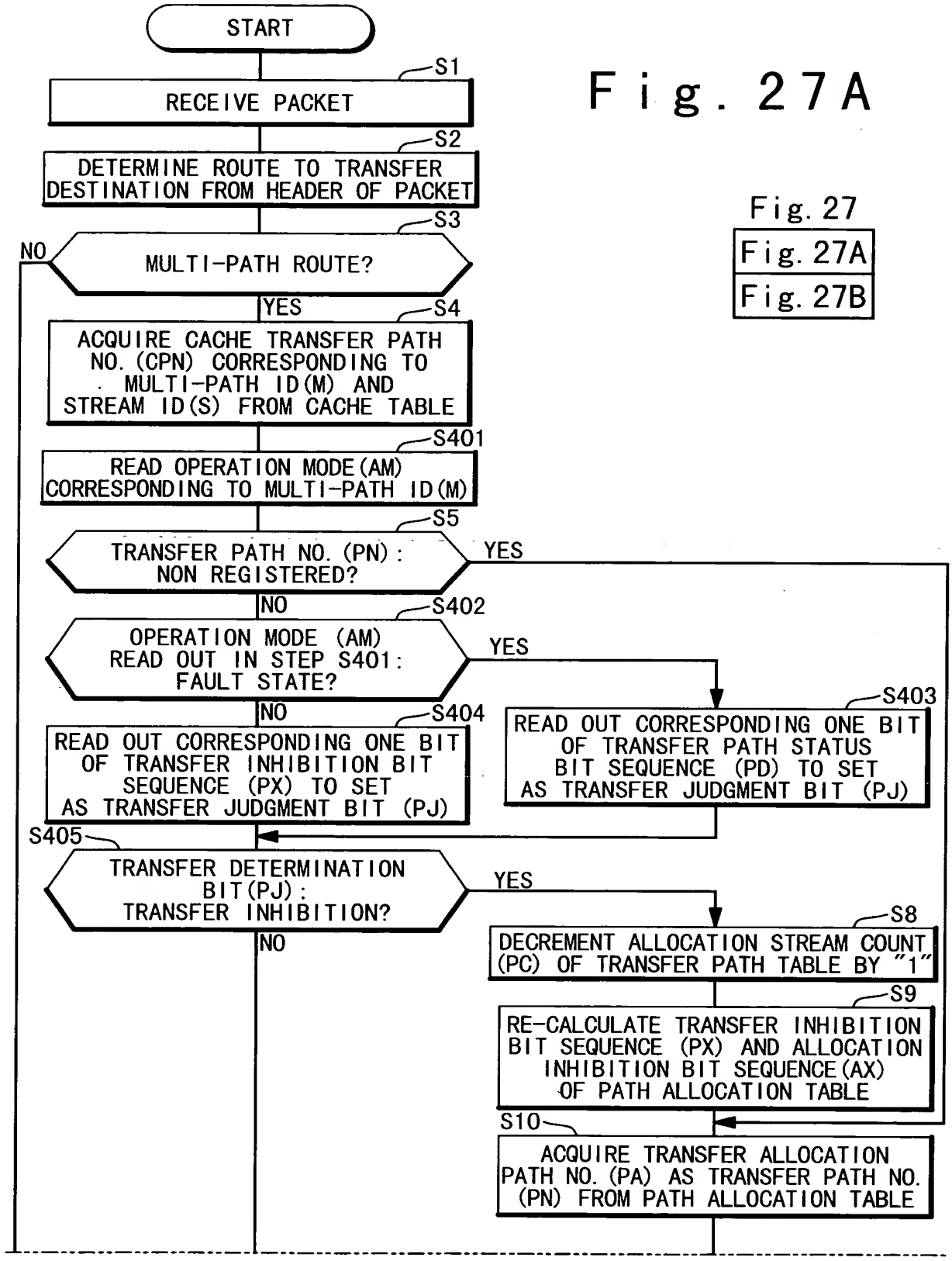


Fig. 27B

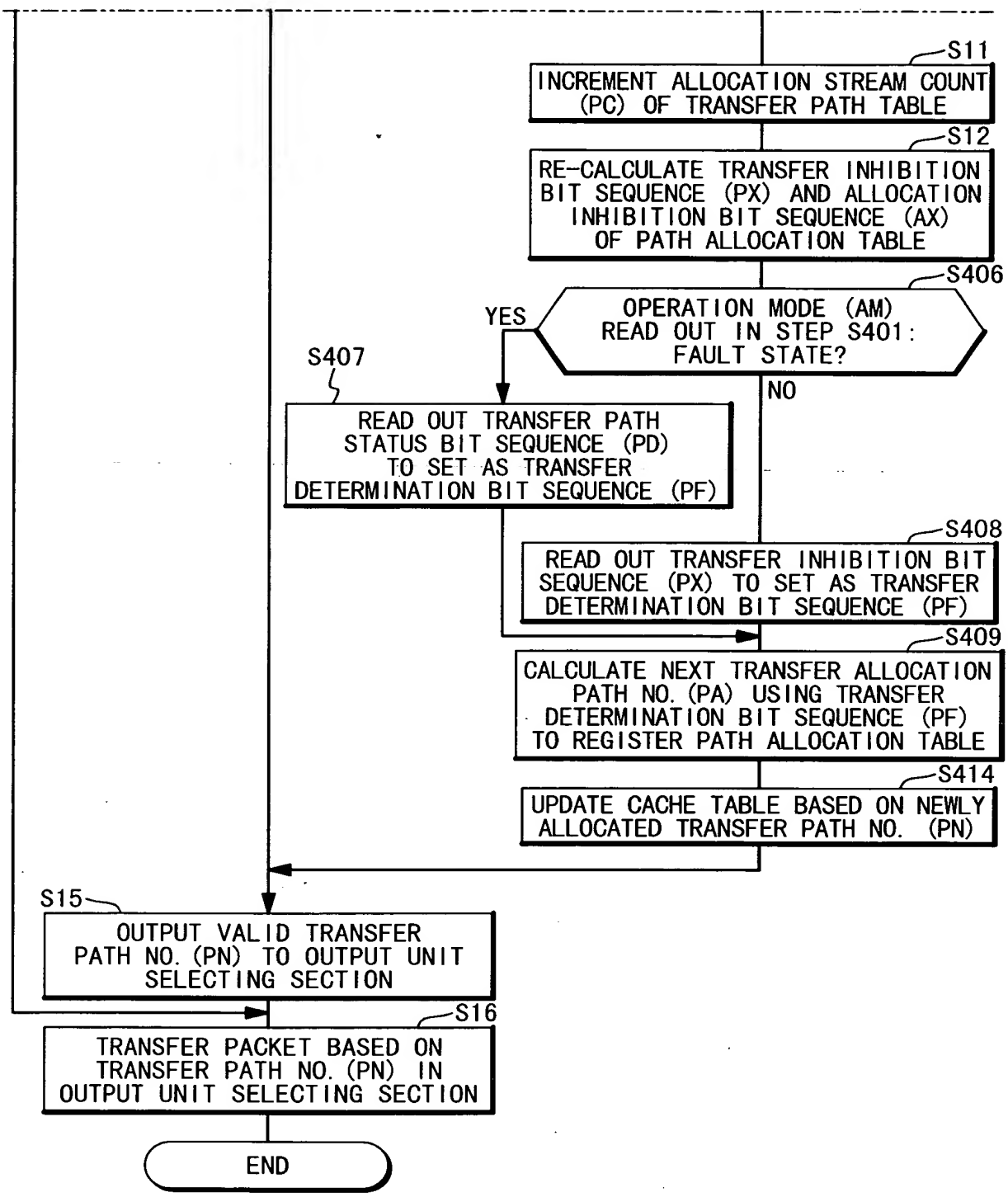

S11
INCREMENT ALLOCATION STREAM COUNT (PC) OF TRANSFER PATH TABLE
S12
RE-CALCULATE TRANSFER INHIBITION BIT SEQUENCE (PX) AND ALLOCATION INHIBITION BIT SEQUENCE (AX) OF PATH ALLOCATION TABLE
S406
OPERATION MODE (AM) READ OUT IN STEP S401: FAULT STATE?
YES
NO
S407
READ OUT TRANSFER PATH STATUS BIT SEQUENCE (PD) TO SET AS TRANSFER DETERMINATION BIT SEQUENCE (PF)
S408
READ OUT TRANSFER INHIBITION BIT SEQUENCE (PX) TO SET AS TRANSFER DETERMINATION BIT SEQUENCE (PF)
S409
CALCULATE NEXT TRANSFER ALLOCATION PATH NO. (PA) USING TRANSFER DETERMINATION BIT SEQUENCE (PF) TO REGISTER PATH ALLOCATION TABLE
S414
UPDATE CACHE TABLE BASED ON NEWLY ALLOCATED TRANSFER PATH NO. (PN)
S15
OUTPUT VALID TRANSFER PATH NO. (PN) TO OUTPUT UNIT SELECTING SECTION
S16
TRANSFER PACKET BASED ON TRANSFER PATH NO. (PN) IN OUTPUT UNIT SELECTING SECTION
END

Fig. 28

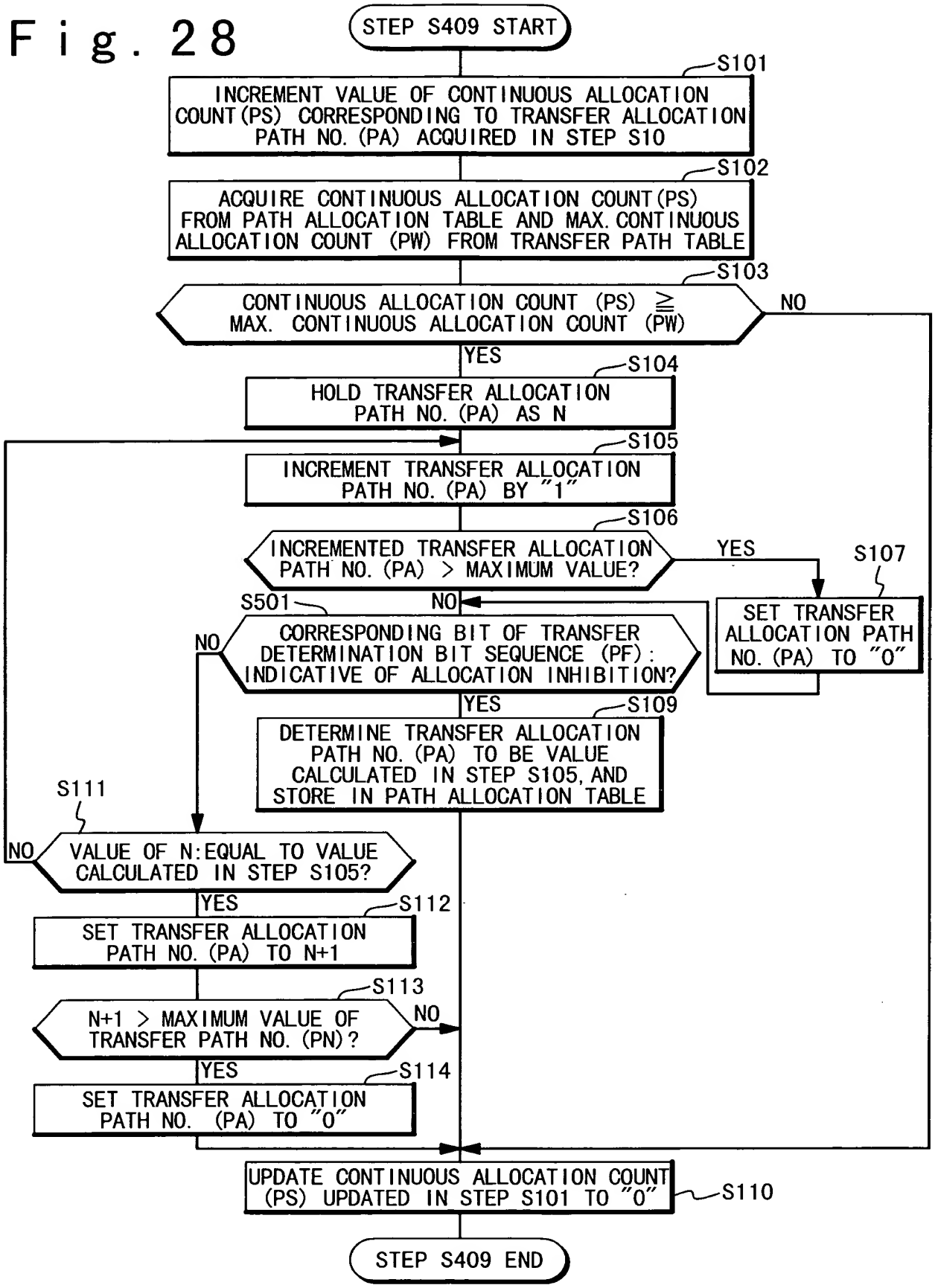

STEP S409 START
S101
INCREMENT VALUE OF CONTINUOUS ALLOCATION COUNT(PS) CORRESPONDING TO TRANSFER ALLOCATION PATH NO. (PA) ACQUIRED IN STEP S10
S102
ACQUIRE CONTINUOUS ALLOCATION COUNT(PS) FROM PATH ALLOCATION TABLE AND MAX. CONTINUOUS ALLOCATION COUNT (PW) FROM TRANSFER PATH TABLE
S103
CONTINUOUS ALLOCATION COUNT (PS) ≧ MAX. CONTINUOUS ALLOCATION COUNT (PW)
NO
YES
S104
HOLD TRANSFER ALLOCATION PATH NO. (PA) AS N
S105
INCREMENT TRANSFER ALLOCATION PATH NO. (PA) BY "1"
S106
INCREMENTED TRANSFER ALLOCATION PATH NO. (PA) > MAXIMUM VALUE?
YES
S107
SET TRANSFER ALLOCATION PATH NO. (PA) TO "0"
S501
NO
CORRESPONDING BIT OF TRANSFER DETERMINATION BIT SEQUENCE (PF): INDICATIVE OF ALLOCATION INHIBITION?
NO
YES
S109
DETERMINE TRANSFER ALLOCATION PATH NO. (PA) TO BE VALUE CALCULATED IN STEP S105, AND STORE IN PATH ALLOCATION TABLE
S111
NO
VALUE OF N:EQUAL TO VALUE CALCULATED IN STEP S105?
YES
S112
SET TRANSFER ALLOCATION PATH NO. (PA) TO N+1
S113
N+1 > MAXIMUM VALUE OF TRANSFER PATH NO. (PN)?
NO
YES
S114
SET TRANSFER ALLOCATION PATH NO. (PA) TO "0"
UPDATE CONTINUOUS ALLOCATION COUNT (PS) UPDATED IN STEP S101 TO "0"
S110
STEP S409 END

Fig. 29

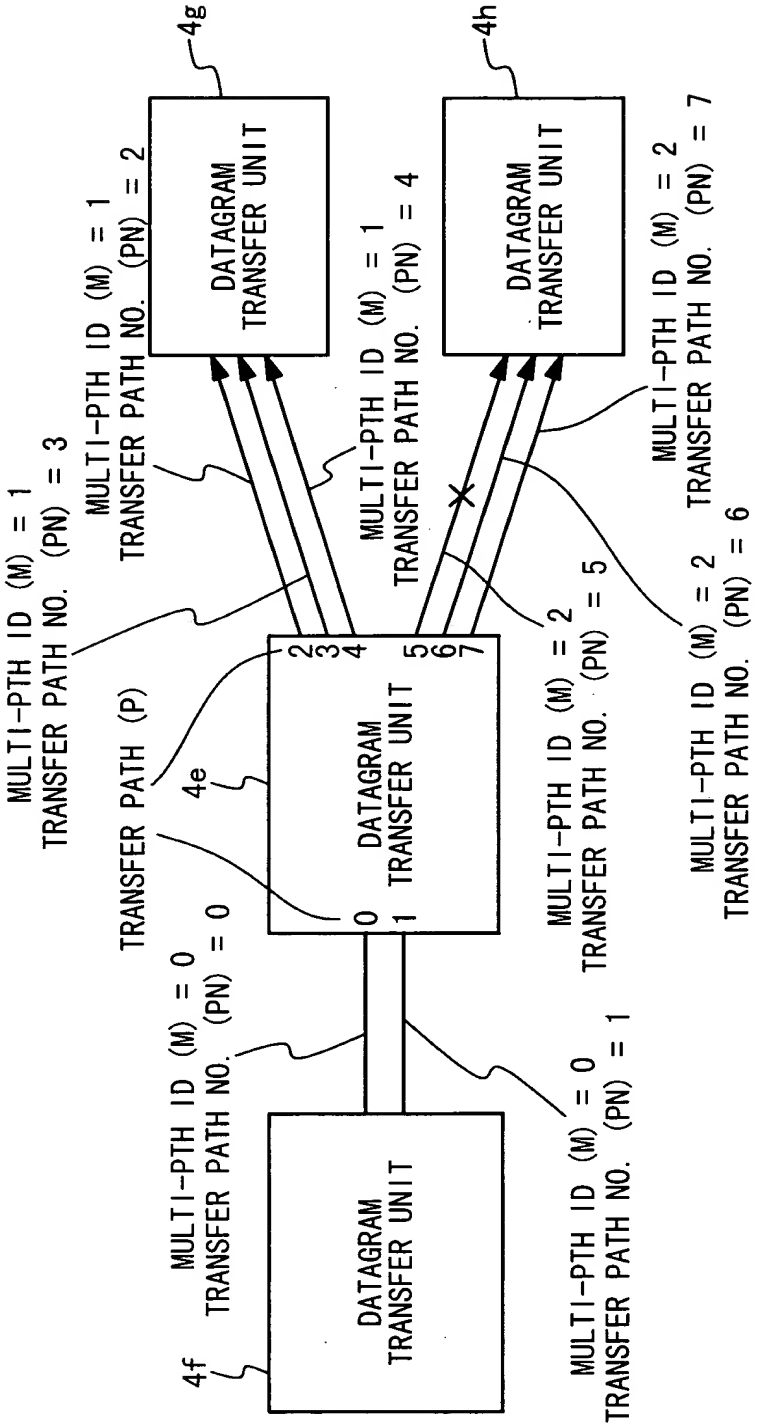
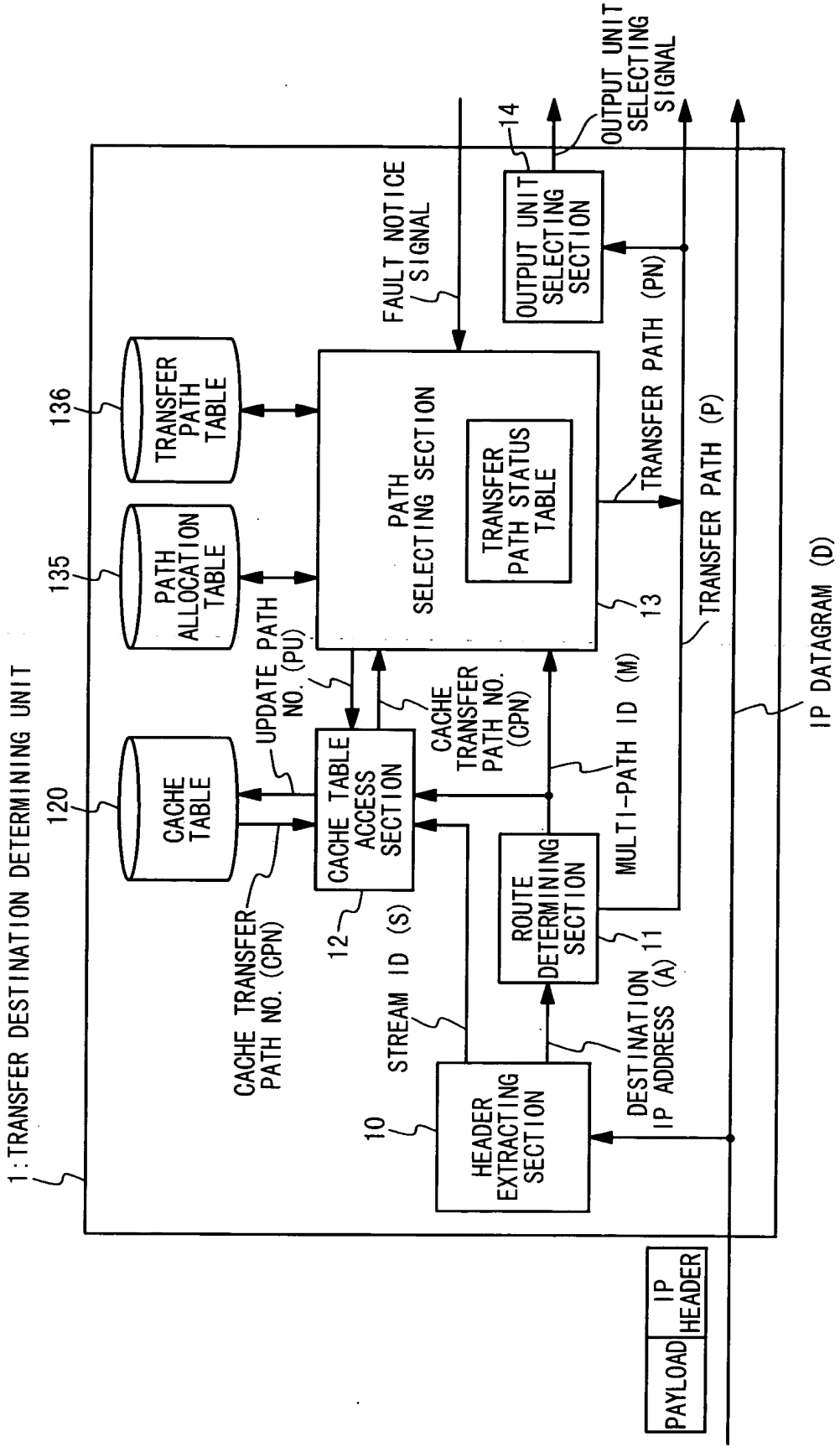

4g
4h
DATAGRAM TRANSFER UNIT
DATAGRAM TRANSFER UNIT
DATAGRAM TRANSFER UNIT
4e
4f
MULTI-PTH ID (M) = 1 TRANSFER PATH NO. (PN) = 3
MULTI-PTH ID (M) = 1 TRANSFER PATH NO. (PN) = 2
MULTI-PTH ID (M) = 1 TRANSFER PATH NO. (PN) = 4
MULTI-PTH ID (M) = 2 TRANSFER PATH NO. (PN) = 7
MULTI-PTH ID (M) = 2 TRANSFER PATH NO. (PN) = 6
MULTI-PTH ID (M) = 2 TRANSFER PATH NO. (PN) = 5
TRANSFER PATH (P)
MULTI-PTH ID (M) = 0 TRANSFER PATH NO. (PN) = 0
MULTI-PTH ID (M) = 0 TRANSFER PATH NO. (PN) = 1
0
1
2
3
4
5
6
7

Fig. 30


1: TRANSFER DESTINATION DETERMINING UNIT
HEADER EXTRACTING SECTION
10
STREAM ID (S)
DESTINATION IP ADDRESS (A)
ROUTE DETERMINING SECTION
11
MULTI-PATH ID (M)
CACHE TABLE ACCESS SECTION
12
CACHE TRANSFER PATH NO. (CPN)
UPDATE PATH NO. (PU)
CACHE TRANSFER PATH NO. (CPN)
CACHE TABLE
120
PATH ALLOCATION TABLE
135
TRANSFER PATH TABLE
136
PATH SELECTING SECTION
TRANSFER PATH STATUS TABLE
13
FAULT NOTICE SIGNAL
TRANSFER PATH (P)
TRANSFER PATH (PN)
OUTPUT UNIT SELECTING SECTION
14
OUTPUT UNIT SELECTING SIGNAL
IP DATAGRAM (D)
PAYLOAD
IP HEADER

JP2001-358760

Fig. 31

135:PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION				
MULTI-PATH ID (M)	USE PATH BIT SEQUENCE (UP)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	11111100	11111100	11111111	0	0
1	11100011	11100011	11111111	0	0
2	00011111	00011111	11111111	0	0

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Fig. 32

136: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION		
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)
0	0	2048	2048	1
	1	2048	2048	1
	2	0	0	0
	3	0	0	0
	4	0	0	0
	5	0	0	0
	6	0	0	0
	7	0	0	0
1	0	0	0	0
	1	0	0	0
	2	1365	1365	1
	3	1365	1365	1
	4	1366	1366	1
	5	0	0	0
	6	0	0	0
	7	0	0	0
2	0	0	0	0
	1	0	0	0
	2	0	0	0
	3	0	0	0
	4	0	0	0
	5	1365	1365	1
	6	1365	1365	1
	7	1366	1366	1

Fig. 33

137:TRANSFER PATH STATUS TABLE

TRANSFER PATH STATUS BIT SEQUENCE (PD)
00000000

Fig. 34

135:PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION				
MULTI-PATH ID (M)	USE PATH BIT SEQUENCE (UP)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	11111100	11111100	11111111	0	0
1	11100011	11100011	11111111	0	0
2	00011111	00011111	11111111	0	0

Fig. 35

137:TRANSFER PATH STATUS TABLE

TRANSFER PATH STATUS BIT SEQUENCE (PD)
00000000

Fig. 36

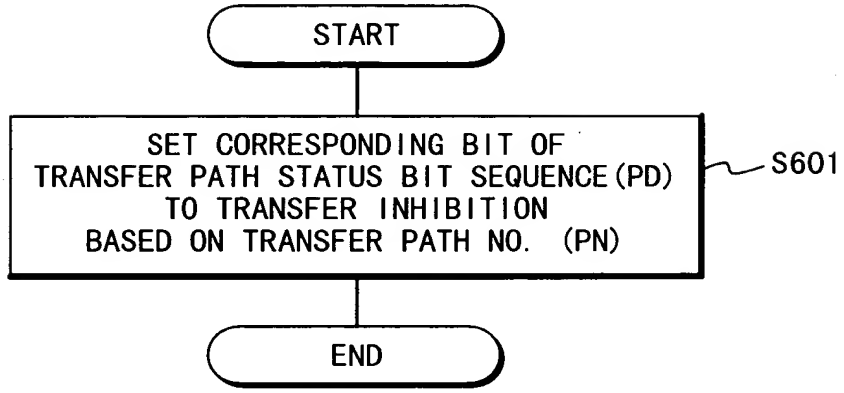
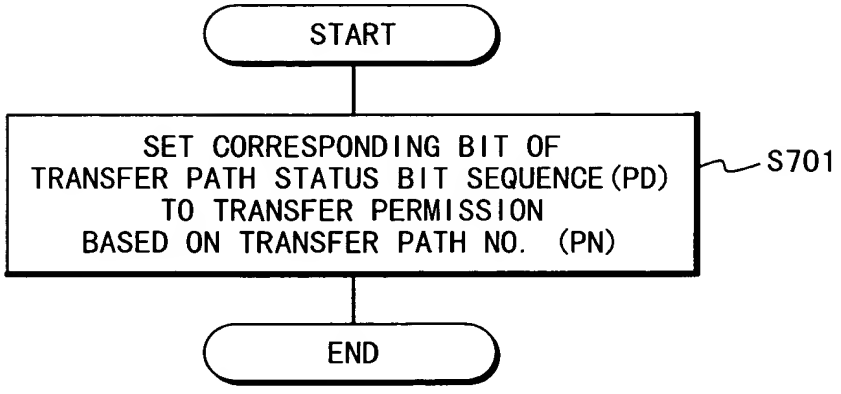

START
SET CORRESPONDING BIT OF TRANSFER PATH STATUS BIT SEQUENCE (PD) TO TRANSFER INHIBITION BASED ON TRANSFER PATH NO. (PN)
S601
END

Fig. 37


START
SET CORRESPONDING BIT OF TRANSFER PATH STATUS BIT SEQUENCE (PD) TO TRANSFER PERMISSION BASED ON TRANSFER PATH NO. (PN)
S701
END

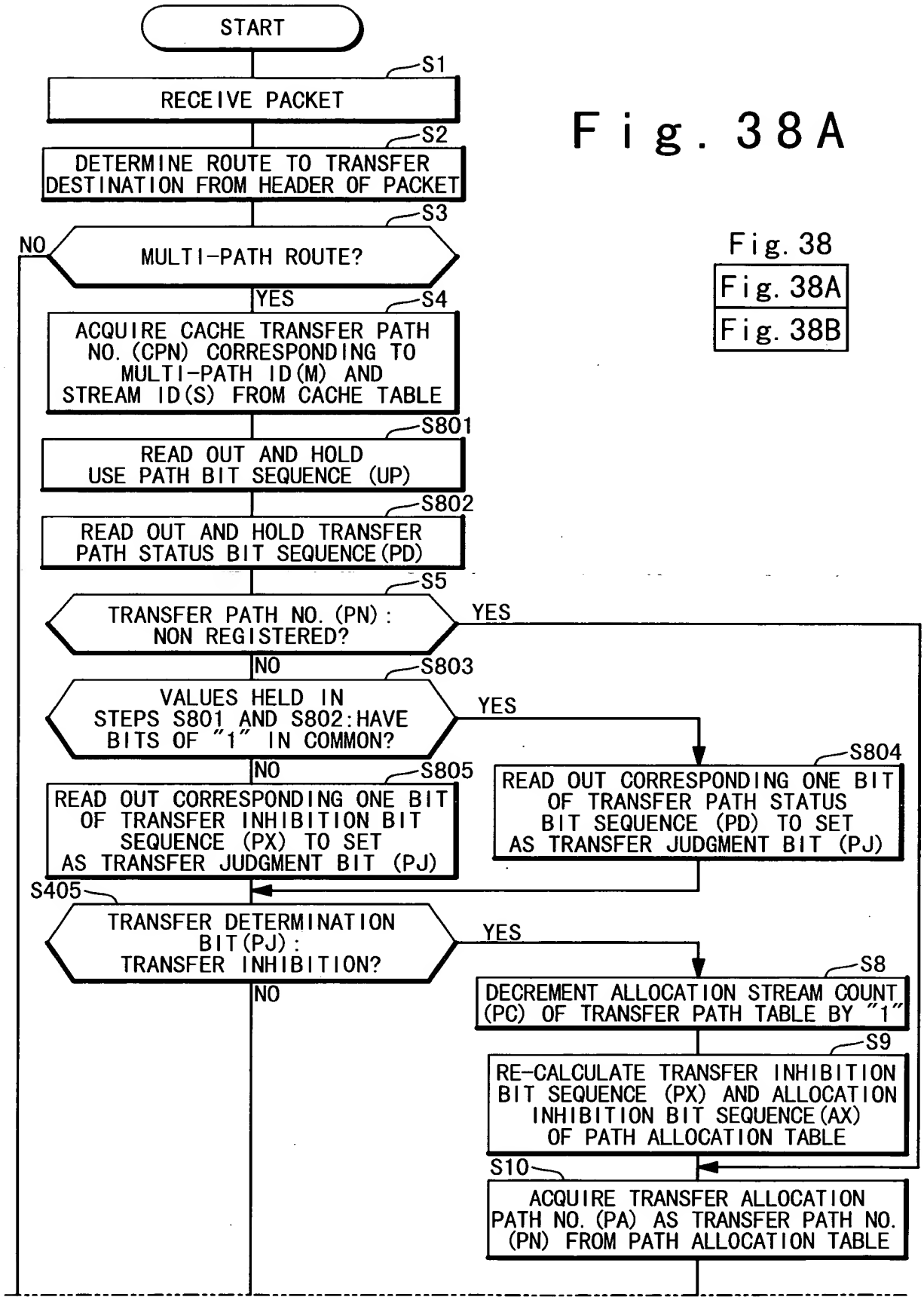


Fig. 38A

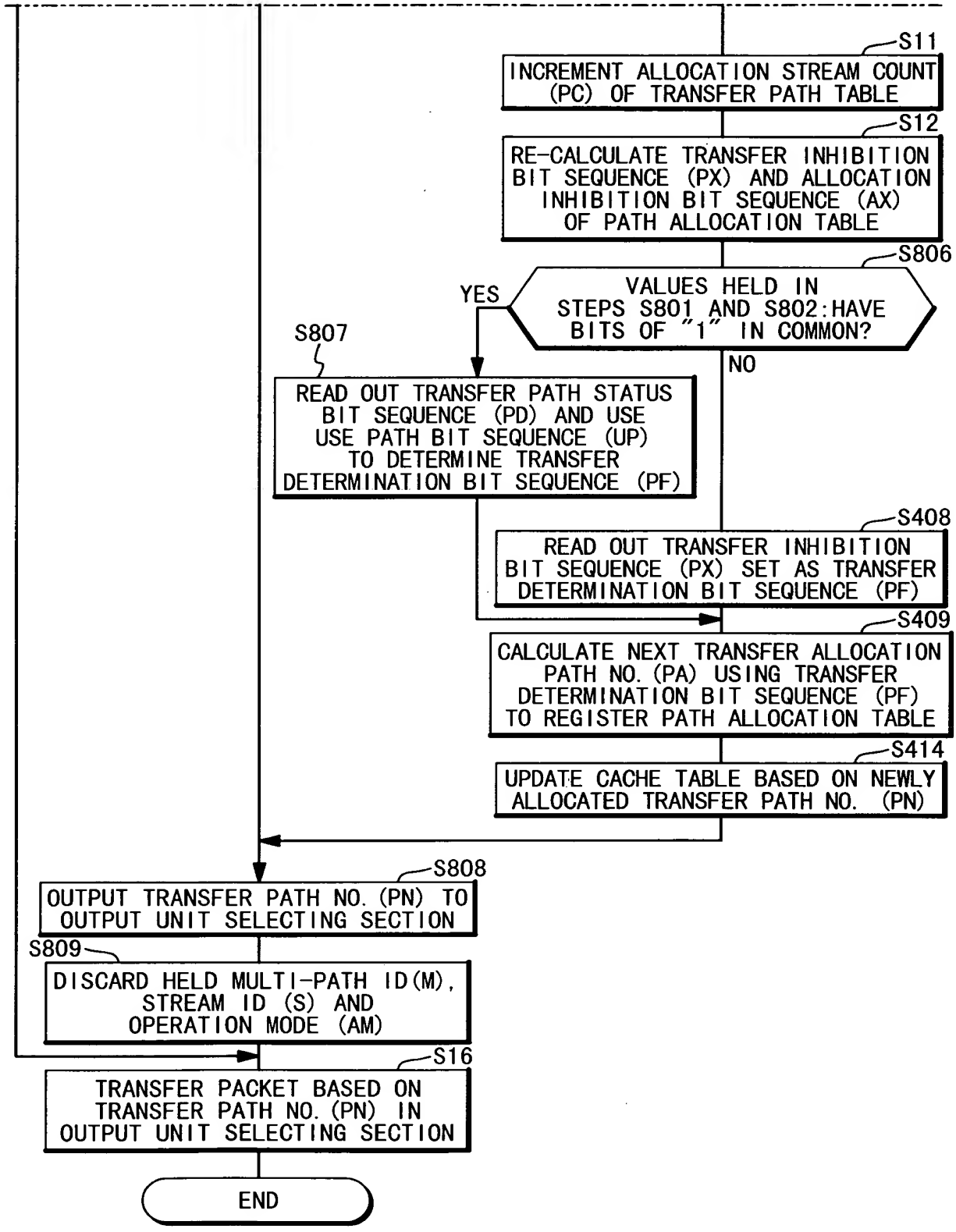
Fig. 38

Fig. 38A

Fig. 38B

0352-0104.030501

Fig. 38B


S11
INCREMENT ALLOCATION STREAM COUNT (PC) OF TRANSFER PATH TABLE
S12
RE-CALCULATE TRANSFER INHIBITION BIT SEQUENCE (PX) AND ALLOCATION INHIBITION BIT SEQUENCE (AX) OF PATH ALLOCATION TABLE
S806
VALUES HELD IN STEPS S801 AND S802: HAVE BITS OF "1" IN COMMON?
YES
NO
S807
READ OUT TRANSFER PATH STATUS BIT SEQUENCE (PD) AND USE USE PATH BIT SEQUENCE (UP) TO DETERMINE TRANSFER DETERMINATION BIT SEQUENCE (PF)
S408
READ OUT TRANSFER INHIBITION BIT SEQUENCE (PX) SET AS TRANSFER DETERMINATION BIT SEQUENCE (PF)
S409
CALCULATE NEXT TRANSFER ALLOCATION PATH NO. (PA) USING TRANSFER DETERMINATION BIT SEQUENCE (PF) TO REGISTER PATH ALLOCATION TABLE
S414
UPDATE CACHE TABLE BASED ON NEWLY ALLOCATED TRANSFER PATH NO. (PN)
S808
OUTPUT TRANSFER PATH NO. (PN) TO OUTPUT UNIT SELECTING SECTION
S809
DISCARD HELD MULTI-PATH ID(M), STREAM ID (S) AND OPERATION MODE (AM)
S16
TRANSFER PACKET BASED ON TRANSFER PATH NO. (PN) IN OUTPUT UNIT SELECTING SECTION
END